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Multilevel Inverter: A Literature Survey on Control Techniques and Topologies

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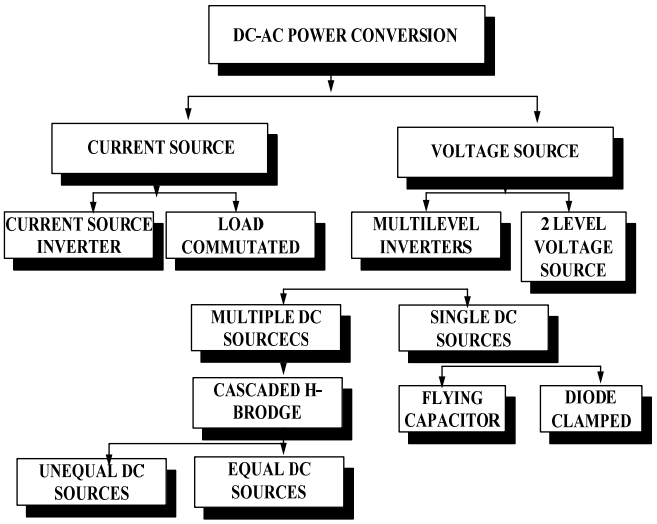
Abstract—*In this study, the main common structure electrical converter topologies and management schemes are reviewed. structure electrical converter topologies (MLIs) area unit progressively being employed in medium and high power applications as a result of their several benefits like low power dissipation on power switches, low harmonic contents and low magnetic force interference (EMI) outputs. the chosen change technique to manage the electrical converter will have a good role on harmonic elimination whereas generating the best output voltage. Intensive studies are performed on carrier-based, sinusoidal, area vector and letter of the alphabet delta PWM ways in open loop management of inverters. the choice of topology and management techniques might vary consistent with power demands of electrical converter.*

1. INTRODUCTION

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [1]. More recent applications have been for power system converters for VAR compensation and stability enhancement [2], Active Filtering [3], High-Voltage motor drive [4], High-voltage DC transmission [5], and most recently for medium voltage Induction motor variable speed drives [6].



Classification of Multilevel converter

The previous approaches inherited the benefit of well-known circuit structures and control methods. However, the newer semiconductors are more expensive, and by going higher in power, other power-quality requirements have to be fulfilled, introducing the need of power filters. The new approach uses the well-known and cheaper semiconductors, but the more complex circuit structures came along with several challenges for implementation and control. Nevertheless, these challenges turned rapidly into new opportunities, since the more complex circuit structures enabled more control degrees of freedom that could be used to improve power conversion in several aspects, especially in relation to power quality and efficiency.[7-10]

2. MULTILEVEL INVERTER CLASSIFIED INTO THREE TYPES

A. Diode clamped multilevel inverter(Neutral Point Clamped Inverter).

B. Flying Capacitor Multilevel Inverter (Capacitor Clamped Inverter).

C. Cascaded H-bridge Multilevel Inverter.

2.1 Diode Clamped Multilevel Inverter[10-12]

Shows a three level diode clamped inverter in which the two series connected capacitors C1 and C2 divide the dc voltage into three output voltage levels van : $V_{dc/2}$,0 and - $V_{dc/2}$ by the switching combination as shown in Table 2.1.The switching state 1 implies the switch is ON whereas state 0 implies that it is OFF. The two diodes D1 and D2 clamp the voltage across the switch to When both S_1 and S_2 are turned ON, the voltage across a and 0 $V_{a0} = V_{dc}$. S_1' blocks the voltage across C_1 and S_2 ' blocks the voltage across C2, D1' balances the voltage sharing between S1' and S2'. The voltage V_{an} is ac whereas voltage V_{a0} is dc. If the output is found between a and 0, then it is a dc-dc converter which has three output voltage levels:$V_{dc,}V_{dc/2}$ and 0. Similarly, Fig. 2.2(b) shows a five level diode clamped converters having four capacitors C1, C2, C3 and C4. Voltage across each capacitor is and each device is required to block a voltage level of $V_{dc/4}$. There are five switch combinations to obtain the output voltage as shown in the Table 2.2

Table 2.1: Switching combination for a three level neutral point clamped inverter

Voltage Van	S1	S2	S1’	S2’
Vdc/2	1	1	0	0
0	0	1	1	0
-Vdc/2	0	0	1	1

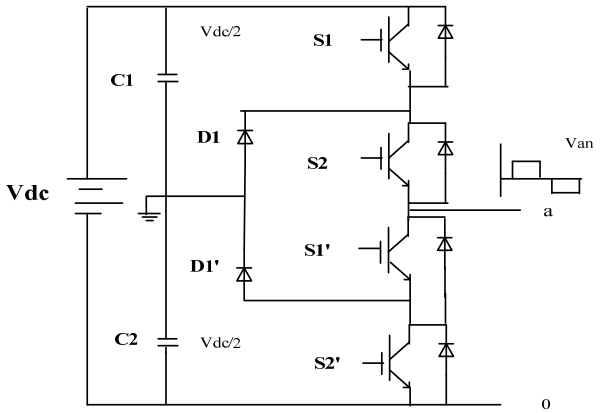


Fig. 2.2: Single Phase Neutral Clamped Multilevel Inverter circuit (a) three level [15]

Table 2.2: Five level Diode Clamped Voltage and Switching States

Output Vao					Switch State			
	S1	S2	S3	S4	S1’	S2’	S3’	S4’
V5=Vdc	1	1	1	1	0	0	0	0
V4=Vdc/4	0	1	1	1	1	0	0	0
V3=Vdc/2	0	0	1	1	1	1	0	0
V2= Vdc/4	0	0	0	1	1	1	1	0
V1=0	0	0	0	0	1	1	1	1

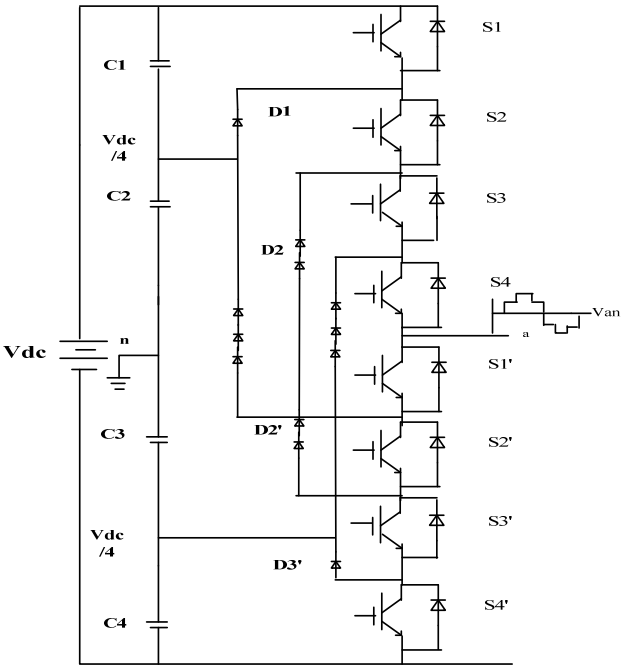


Fig. 2.2: Single Phase Neutral Clamped Multilevel Inverter circuit (b) five level[15]

2.2 Capacitor Clamped Multilevel Inverter[13-15]

Fig.2.2(a) shows a three level capacitor clamped inverter. Here instead of diodes, capacitors are used to clamp the device voltage to one capacitor voltage level. The voltage across a and 0 van has three voltage levels $V_{an:}$ $V_{dc}/2$, 0, $-V_{dc}/2$ by the switching combination as shown in Table 2.3.The switching state ‘1’ denotes that switch is ON and state ‘0’ denotes that switch is OFF. There are two possible combinations to obtain the voltage level $-V_{dc}/2$.

Table 2.3: Switching Combination for Three Level Capacitor Clamped Inverter

Voltage Van	S1	S2	S1’	S2’
Vdc/2	1	1	0	0
0	0	0	1	1
-Vdc/2	1	0	1	0
	0	1	0	1

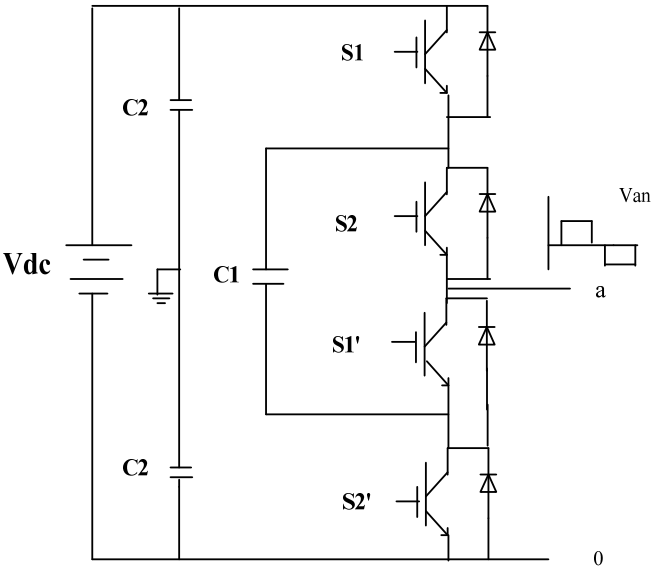


Fig. 2.3: Single Phase Capacitor Clamped Multilevel Inverter circuit (a) three level

Table 2.3: Switching Combination for Three Level Capacitor Clamped Inverter

Output Vao			Switch State					
	S1	S2	S3	S4	S1’	S2’	S3’	S4’
V5=Vdc	1	1	1	1	0	0	0	0
V4=Vdc/4	0	1	1	1	1	0	0	0
V3=Vdc/2	0	0	1	1	1	1	0	0
V2= Vdc/4	0	0	0	1	1	1	1	0
V1=0	0	0	0	0	1	1	1	1

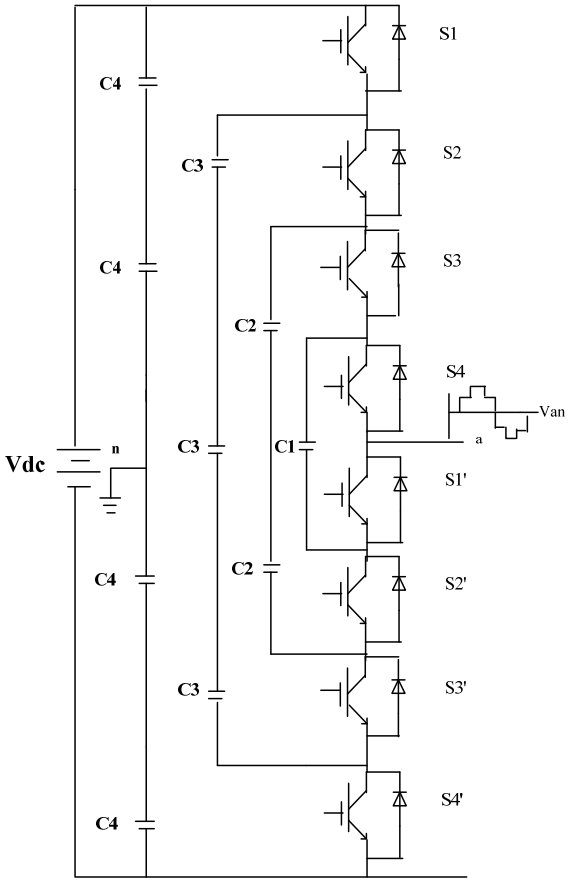


Fig. 2.3: Single Phase Capacitor Clamped Multilevel Inverter circuit (b) five level

2.3 Cascaded H-Bridge Multilevel Inverter[16-18]

Fig. 2.5 shows a phase leg of a five level cascaded inverter. It consists of two H-Bridge inverter units with two isolated and equal DC sources. When switches S11 , S21 and switches S12 , S22 conduct, the output voltage of the H Bridges H1 and H2 is $V_{H1} + V_{H2} = E$ and the resultant inverter phase voltage is

$$V_{AN} = V_{H1} + V_{H2} = 2E$$

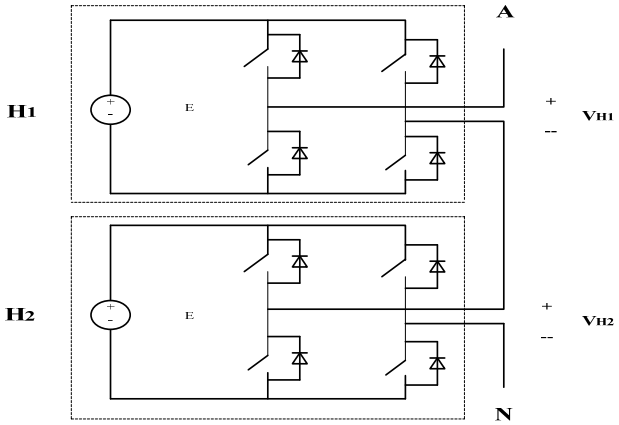


Fig. 2.5: Cascaded multilevel inverter topology

Table 2.5: Comparison of component requirement per leg of three types of multilevel inverter[28]

Converter Type	Diode Clamped	Flying Capacitors	Cascaded H-Bridge
Main switching devices	(m-1)*2	(m-1)*2	(m-1)*2
Main diodes	(m-1)*2	(m-1)*2	(m-1)*2
Clamping diodes	(m-1)* (m-2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)* (m-2)/2	0

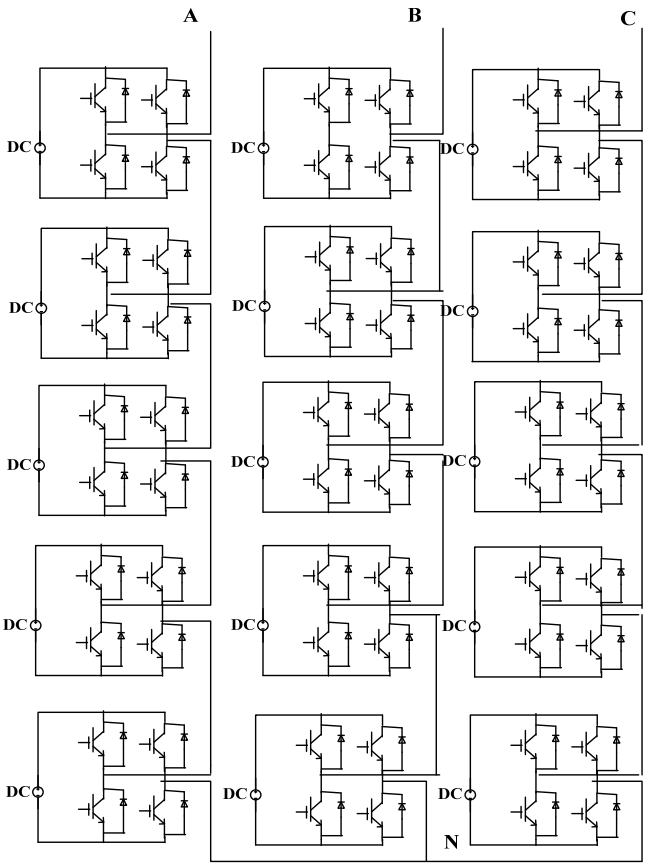


Fig. 2.5: An eleven level cascaded inverter

3. MODULATION TOPOLOGIES OF MULTILEVEL INVERTER [20-25]

Switching frequency, modulation techniques are broadly divided into 2 parts as fundamental switching frequency and high switching frequency pulse width modulation (PWM). Space vector control and selective harmonic elimination (SHE) modulation techniques come under fundamental switching frequency.

- **In Phase disposition (IPD)**:- In this modulation technique, all the carriers are in phase and reference wave is 3-phase sinusoidal wave.
- **Phase opposition disposition (POD)**:- In this type of modulation technique, the carriers above the sinusoidal reference zero point are in phase, but shifted by 180o out of phase with those below the zero reference point.
- **Alternative phase opposition disposition (APOD)**:- In this type of modulation technique, each carrier is phase shifted by 180o from its adjacent carrier.

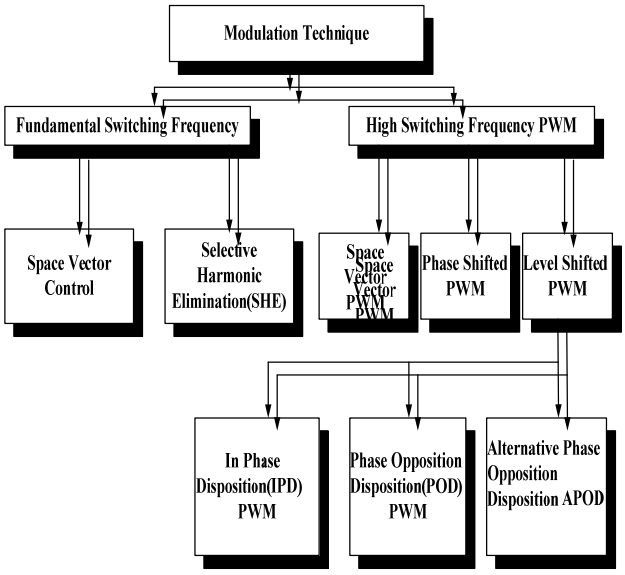


Fig. 3.1: Classification of Different Types of Modulation Technique

4. CONCLUSION

Based on the survey of standard structure electrical converter topologies given within the previous sections, general and unsymmetrically well-grooved H-MLIs are additionally reviewed during this paper. Several new hybrid topologies will be designed through the mixtures of 3 main MLI topologies. Besides the mix of topologies, the trade-offs in MLI structures will be dealt by victimisation AH-MLIs that's shaped victimisation completely different DC supply levels in electrical converter cells. yet, standard PWM methods that generate switch frequency at fundamental don't seem to be acceptable for MLIs thanks to switch devices of the upper voltage modules would got to operate at high frequencies solely throughout some inverting instants.

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